REMARKS

The Office Action of June 4, 2004 has been carefully considered. Reconsideration in view of the present remarks is respectfully requested.

Claims 12 and 13 were rejected as being anticipated by the Admitted Prior Art (APA) and as being unpatentable over APA in view of Barry. Claim 2, 4, 10 and 11 were rejected as being unpatentable over APA in view of Barry. Claim 5 was rejected as being unpatentable over APA in view of Barry and further in view of Dias.

Considering first the rejection of claims 12 and 13, claim 12 recites in part "generating within an external tester test vectors for the logic circuitry, *using a programmable test vector generator*." Figure 1 of the specification does not illustrate any such use of a programmable test vector generator, nor does Figure 2 of the specification. Accordingly, claim 12 is not anticipated by APA. Claim 13 depends on claim 12 and therefore is also not anticipated, for like reasons.

Again in relation to claim 12, the rejection states in part "[I]t would have been obvious...to use a test vector pattern generator in an embodiment as described by Spec in Figure 1 and lines 5-10 of page 4...to prevent from having to use a large test memory as suggested by Specs in lines 10-14 of page 1." The cited passage, however, relates to test systems for *memory ICs*. There is no suggestion of the use of a programmable test vector generator for *logic circuitry* as in claim 12 and dependent claim 13.

Considering next the rejection of claims 2, 4, 10 and 11, the same *non-sequitur* used in the rejection of claim 12, above, is again used in rejecting claim 10. Nothing in the specification can be construed as suggesting the use of a programmable test vector generator for *logic circuitry* as in claim 10 and dependent claims 4 and 5. Similarly in relation to claim 11, there is no suggestion in the prior art of the rejection to substitute a programmable test vector generator for the vector memory of Figure 1 for the purpose of

testing logic circuitry, and no motivation to combine the sisr of Barry, which relates to the testing of *memory circuits*, into the *logic IC* of Figure 1.

Accordingly, claims 10-12 are believed to patentably define over the cited references.

Dependent claims 2, 4, 5 and 13 are also believed to add novel and patentable subject matter to their respective independent claims. Withdrawal of the rejection and allowance of claims 2, 4, 5 and 10-13 is respectfully requested.

Respectfully submitted,

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